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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,392	12/02/2003	Hiromichi Kumakura	31904-3	5617
7590	04/05/2005			
Mitchell P. Brook, Esq. LUCE, FORWARD, HAMILTON & SCRIPPS LLP Suite 200 11988 El Camino Real San Diego, CA 92130			EXAMINER WARREN, MATTHEW E	
			ART UNIT 2815	PAPER NUMBER
DATE MAILED: 04/05/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,392	KUMAKURA ET AL. 	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 27 December 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7, 14-21, 29 and 30 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-3, 5-7, 14-16, 18-21, 29 and 30 is/are rejected.
 7) Claim(s) 4 and 17 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the Amendment filed on December 27, 2004.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 30 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim contains the limitation "..., containing the surface corresponding to the areas on which said wiring layer is provided." The grammatical structure makes it difficult to determine if the limitation refers specifically to the metal layer or the third insulation layer. For purposes of examination, the limitation will be interpreted to mean that "..., said third insulation film also containing the surface corresponding to the areas on which said wiring layer is provided." Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6, 7, 14-16, 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga et al. (US 6,559,548 B1) in view of Gansauge et al. (US 5,010,389).

In re claim 1, Matsunaga et al. shows (fig. 1) a semiconductor device comprising: a semiconductor base (10), and a first insulation film (11) which is provided on said semiconductor base. Matsunaga does not specifically disclose that the first insulation material is made of a silicon material, but such a limitation is not patentably distinguishable over the cited art because silicon oxide is a well known insulating material used in the technology of semiconductors. The applicant's specification discloses (pg. 2, lines 4-10 and fig. 2) that silicon oxide is typically used as a first insulating film in conjunction with a stack of insulating films. A second insulation film (13) which is provided on said first insulation film, is made of an organic material and is thicker than said first insulation film. A third insulation film (14), which is provided on said second insulation film, is made of a silicon material and is thinner than said second insulation film. A metal wiring layer (20) is provided on said third insulation film, wherein a current flows between said wiring layer and an external terminal (23). Matsunaga does not show that the wiring layer is grown on a seed layer which is provided on the third insulating layer and forms a wiring layer with the seed layer. However, Gansauge et al. shows (fig. 4) a contact for a semiconductor device having an upper insulation film (12) and a seed layer (20) provided on the upper insulation layer. A metal layer (34) is grown on the seed layer and forms a wiring layer with the seed layer. With this configuration, the addition of the seed layer adheres to the surface of the insulation film,

prevents oxidation and diffusion, and improves the contact and conductive capability. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wiring structure of Matsunaga by using a seed layer for electro-plating a subsequent wiring layer as taught by Gansauge et al. to adhere the wiring layer to the surface of the insulation film, prevent oxidation and diffusion, and improve the contact and conductive capability.

In re claim 2, Matsunaga shows (fig. 9) an alternate embodiment in which a fourth insulation film (96c) is provided between an underlying insulation film (96b) and a wiring layer (98b) so as to cover an entire surface of underlying insulation film and is made of an organic material (col. 11, 25-40)

In re claim 3, Matsunaga shows (fig. 9) an alternate embodiment in which a fifth insulation film (97) is provided between said fourth insulation film (96c) and said wiring layer (98b) and is made of a silicon material (col. 11, lines 25-40).

In re claims 6 and 7, Matsunaga shows (fig. 1) that said wiring layer is a metal wiring layer that constitutes a metal pad (20) which is connected to said external terminal (23), and/or a metal wire through which the current flows via said metal pad.

In re claim 14, Matsunaga et al. shows (fig. 1) a semiconductor device comprising: a semiconductor base (10), and a first insulation film (11) which is provided on said semiconductor base. Matsunaga does not specifically disclose that the first insulation material is made of a silicon material, but such a limitation is not patentably distinguishable over the cited art because silicon oxide is a well known insulating

material used in the technology of semiconductors. The applicant's specification discloses (pg. 2, lines 4-10 and fig. 2) that silicon oxide is typically used as a first insulating film in conjunction with a stack of insulating films. A second insulation film (13) which is provided on said first insulation film, is made of an organic material and is thicker than said first insulation film. A third insulation film (14), which is provided on said second insulation film, is made of a silicon material and is thinner than said second insulation film. The third insulation film is silicon nitride which naturally has a moisture resistant property. A metal wiring layer (20) is provided on said third insulation film, wherein a current flows between said wiring layer and an external terminal (23). Matsunaga does not show that the wiring layer is grown on a seed layer which is provided on the third insulating layer and forms a wiring layer with the seed layer. However, Gansauge et al. shows (fig. 4) a contact for a semiconductor device having an upper insulation film (12) and a seed layer (20) provided on the upper insulation layer. A metal layer (34) is grown on the seed layer and forms a wiring layer with the seed layer. With this configuration, the addition of the seed layer adheres to the surface of the insulation film, prevents oxidation and diffusion, and improves the contact and conductive capability. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wiring structure of Matsunaga by using a seed layer for electro-plating a subsequent wiring layer as taught by Gansauge et al. to adhere the wiring layer to the surface of the insulation film, prevent oxidation and diffusion, and improve the contact and conductive capability.

In re claim 15, Matsunaga shows (fig. 9) an alternate embodiment in which a fourth insulation film (96c) is provided between a third underlying insulation film (96b) and said wiring layer (98b) so as to cover an entire surface of said third insulation film in order to prevent said third insulation film from being damaged.

In re claim 16, Matsunaga shows (fig. 9) an alternate embodiment in which a fifth insulation film (97) which is provided between said fourth insulation film (96c) and a wiring layer (98b) . The fifth insulation film is a silicon nitride passivation material (col. 11, lines 25-40) that naturally functions as an adhesive layer.

In re claim 18, Matsunaga shows does not specifically disclose that said fourth insulation film functions as an adhesive layer for preventing separation of said wiring layer. However, because the materials and structure is the same as the instant invention, the fourth insulation layer of Matsunaga inherently functions as an adhesive layer.

In re claims 20 and 21, Matsunaga shows (fig. 1) that said wiring layer is a metal wiring layer that constitutes a metal pad (20) which is connected to said external terminal (23), and/or a metal wire through which the current flows via said metal pad.

Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga et al. (US 6,559,548 B1) in view of Gansauge et al. (US 5,010,389) as applied to claims 1 and 2 above, and further in view of Noda (JP 2001-177115 A).

In re claim 5, neither reference discloses that said fourth insulation film is made of polybenzoxazole resin. Noda discloses (abstract) that an organic material may be

formed of polybenzoxazole resin to form a reliable semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the organic material of the Matsunaga and Gansauge by using polybenzoxazole resin as taught by Noda to provide a highly reliable semiconductor device.

Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga et al. (US 6,559,548 B1).

In re claims 29 and 30, Matsunaga et al. shows (fig. 1) a semiconductor device comprising: a semiconductor base (10), and a first insulation film (11) which is provided on said semiconductor base. Matsunaga does not specifically disclose that the first insulation material is made of a silicon material, but such a limitation is not patentably distinguishable over the cited art because silicon oxide is a well known insulating material used in the technology of semiconductors. The applicant's specification discloses (pg. 2, lines 4-10 and fig. 2) that silicon oxide is typically used as a first insulating film in conjunction with a stack of insulating films. A second insulation film (13) which is provided on said first insulation film, is made of an organic material and is thicker than said first insulation film. A third insulation film (14), which is provided on said second insulation film, is made of a silicon material and is thinner than said second insulation film. A metal wiring layer (20) is provided on said third insulation film, being prevented from separation over an entire region of the semiconductor device by an adhesion of said third insulation film which is sandwiched between said wiring layer and

said second insulation film, wherein a current flows between said wiring layer and an external terminal (23). Furthermore, as recited in claim 30, Matsunaga shows that metal layer (20) which is patterned to form a wiring layer on said third insulation film, wherein a current flows between said wiring layers and an external terminal (23), said third insulation film having sufficient remaining thickness left by the patterning of said metal layer for covering substantially an entire surface of said second insulation film, the third insulation film containing the surface corresponding to the areas on which said wiring layer is provided.

Allowable Subject Matter

Claims 4 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-7 and 14-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
April 3, 2005

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER